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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
FIS920030371US1

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Application Number	Filed
10/708,378	02/27/2004

First Named Inventor
Zhu

Art Unit	Examiner
2818	N. Ngo

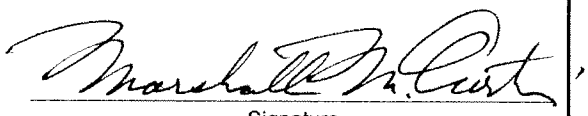
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 33,138
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____



Signature

Marshall M. Curtis
Typed or printed name

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Telephone number

December 11, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Tradeamrk Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Huilong Zhu et al.
Serial No.: 10/708,378
Filed: February 27, 2004
For: HYBRID SOI/BULK SEMICONDUCTOR TRANSISTORS

Conf. No.: 2377
Group Art Unit: No.: 2818
Examiner: N. Ngo

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

ATTACHMENT TO PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This Pre-Appeal Brief Request for Review is being concurrently filed with a Notice of Appeal. A check is attached to satisfy the fees for the Notice of Appeal. If any additional fees are required to satisfy the fees due for the Notice of Appeal or to gain entry and consideration of this Pre-Appeal Brief Request for Review, the Commissioner is authorized to charge Attorney's Deposit Account 50-2041 (Whitham, Curtis, Christofferson & Cook).

The Invention

The invention is a transistor structure which provides an alternative to several different types of known structures that have recently been developed to maintain acceptable transistor performance as transistor designs have been scaled to small sizes and which largely avoids the drawbacks associated with each of these known structures. For example, the invention provides for limitation of the transistor channel depth previously achieved using SOI and UT-SOI structures but can be formed on much less expensive bulk semiconductor substrates, provides for electrical contact to the channel region to avoid floating body effects characteristic of SOI transistors, avoids increased channel resistance also characteristic of SOI transistors and avoids a need for raised source/drain (RSD)

structures (associated with the deleterious effects of increased capacitance and extension implants located too close to the gate) to reduce source and drain resistance by providing increased source and drain depth in the substrate and the like as detailed in paragraphs [0003] to [0010] of the application. The invention also provides a structure in which a dual gate transistor can be formed and the transistor channels may be stressed by a film in the substrate to control transistor carrier mobility which avoids numerous problems such as chip curling or cracking associated with known stressed film structures formed over the transistors.

The invention provides these and other unexpected advantages and meritorious effects by providing a transistor structure in which a film is developed within the substrate which has a discontinuity precisely aligned to the gate structure of the transistor and using different materials for the film and at the discontinuity. The three exemplary disclosed preferred embodiments represented in Figures 2 - 8, 9 - 19 and 20 - 25B, respectively, share the features of:

> "a gate structure formed on said surface of said layer of semiconductor material, and
>
> "a discontinuous film of material within said layer of semiconductor material and having a discontinuity aligned to said gate structure" (claims 1 and 11, upon entry of the amendment presented November 9, 2006, or "a discontinuity having an edge which is located in a position defined by an edge [of] said gate structure" as in claim 21).

The accuracy of the alignment of the discontinuity with the gate structure is relatively critical to the electrical properties and characteristics of the transistors and, if the discontinuity is aligned to the gate, high accuracy of alignment with high repeatability can be achieved with substantial process simplification, reduced process criticality and substantially increased flexibility of design, applicability and material choice.

Errors and Omissions

It is believed that the errors and omissions in the final action can best be appreciated by a brief review of the prosecution history of the application. Original claims 1 and 11 of this application recited the alignment as "a discontinuity aligned with said gate structure". In the first action on the merits of the elected device claims, the Examiner principally relied upon Krivokapic et al. which discloses a transistor structure which resembles the first embodiment of the invention in some respects including the inclusion of an insulating film having a discontinuity and the placement of a gate structure generally above the discontinuity. However, as is evident from Figures 1 - 5a and the discussion in column 2, lines 34 - 59, of Krivokapic et al., the insulating film and discontinuity are developed prior to formation of the gate structure 42 which is later positioned generally in the center between isolation areas 24 and nickel spacers 38 (where amorphous silicon 40 is deposited) by re-crystallization using very specific and unique metallurgy (forming a nickel silicide gate) and only indirectly aligned with the discontinuity by patterning the intended gate *area* 22 relative to the isolation structures 24 as shown in Figure 1 and which is removed to form discontinuity 28. The recited alignment was argued to distinguish from Krivokapic et al. by virtue of the recited of alignment of the discontinuity *with* the gate structure. The Examiner dismissed this argument by asserting a product-by-process analysis, thus admitting the difference in process but asserting similarity of the result.

In response, it was argued that the product-by-process analysis was inappropriate and erroneous and significant differences in the products was demonstrated as well as by amending the claim recitations of the alignment to "formed in alignment with" to emphasize that Krivokapic et al. disclosed an opposite process in which the discontinuity was formed prior to the gate and thus taught directly away from the claimed invention. The Examiner, nevertheless maintained the product-by-process analysis and, in response, claims 21 - 25 were added to recite that *edges* of the discontinuity were aligned with *edges* of the gate as further emphasis of the arguments previously made but which were similarly dismissed by the Examiner as well. The present "aligned to" language presented

in the amendment of November 9, 2006, which the Examiner has indicated will be entered for Appeal, has evidently, but without further comment in the Advisory Action of November 29, 2006, not been found persuasive.

It is respectfully pointed out that a product-by-process analysis merely recognizes that a so-called product-by-process claim is a claim to the product and serves to shift the burden of proof of significant differences in the product to Applicant. It has been repeatedly pointed out that *none* of the versions of the alignment recitation used over the course of the prosecution of this application amount to a method or process recitation much less one that would justify the application of a product-by-process analysis any more than a recitation of "element B located adjacent to element A" is a method or process recitation.

Further, even if, *arguendo*, a product-by-process analysis is justified, it is respectfully submitted that Applicant has clearly met the burden of demonstrating significant differences in the product in that 1.) correct and accurate alignment of the gate and the discontinuity is guaranteed in the invention whereas, in Krivokapic et al. it is not and the alignment is only approximate and provided in an indirect manner which increases the likelihood of misalignment; 2.) even if the gate structure of Krivokapic is located in the correct position, there appears to be no mechanism in Krivokapic et al. for accurately controlling the geometry of the edges of the resulting gate structure as provided by the invention and, in fact, gate 42 is depicted in Krivokapic et al. as being irregular in shape in Figures 5a and 5b; 3.) the invention can be applied to any transistor design and transistor manufacturing process including SOI and bulk semiconductor devices whereas the process required in Krivokapic et al. appears to limit design flexibility, particularly in regard to source and drain structure geometry and does not appear to be capable of being scaled to small sizes and the film discontinuity cannot be sub-lithographic is dimensions as can be achieve by the present dimensions as the invention provides, and 4.) the invention provides a structure which can be formed of virtually any semiconductor material whereas Krivokapic et al. relies on very specific metallurgy and does not teach, suggest or even recognize a need for adjustment of carrier mobility by stressing of the channel, if such an effect is even

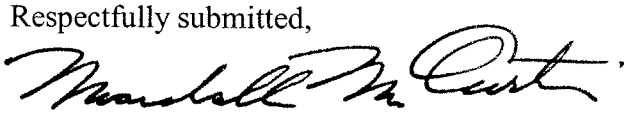
possible since, in Krivokapic et al., the channel 34 must be epitaxially grown over the film 30.

Accordingly, it is respectfully submitted that Krivokapic et al. does not anticipate any claim in the application, particularly since, as the Examiner effectively admits, it does not answer the recitation of the alignment of the discontinuity and does not, in combination with Bae, provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness of any claim. Likewise, it is respectfully submitted that the various recitations of alignment of the film discontinuity to the gate do not justify, much less require a product-by-process analysis of the claims and such analysis has been improperly utilized by the Examiner to colorably justify ignoring of substantive *structural* recitations which directly support unexpected advantages and meritorious effects not available from the prior art, particularly Krivokapic et al. and/or Bae and even if such an analysis were so justified, the differences provided by the invention which have been demonstrated by Applicant are clearly sufficient to shift the burden of making a *prima facie* demonstration of anticipation or obviousness back to the Examiner; to which the Examiner has not substantively responded. Therefore, it is respectfully submitted that the grounds of rejection asserted by the Examiner are clearly in error and untenable.

Conclusion

In view of the above, it is requested that the position of the Examiner be reviewed, that the rejections be withdrawn, and that the application be passed to issue.

Respectfully submitted,



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